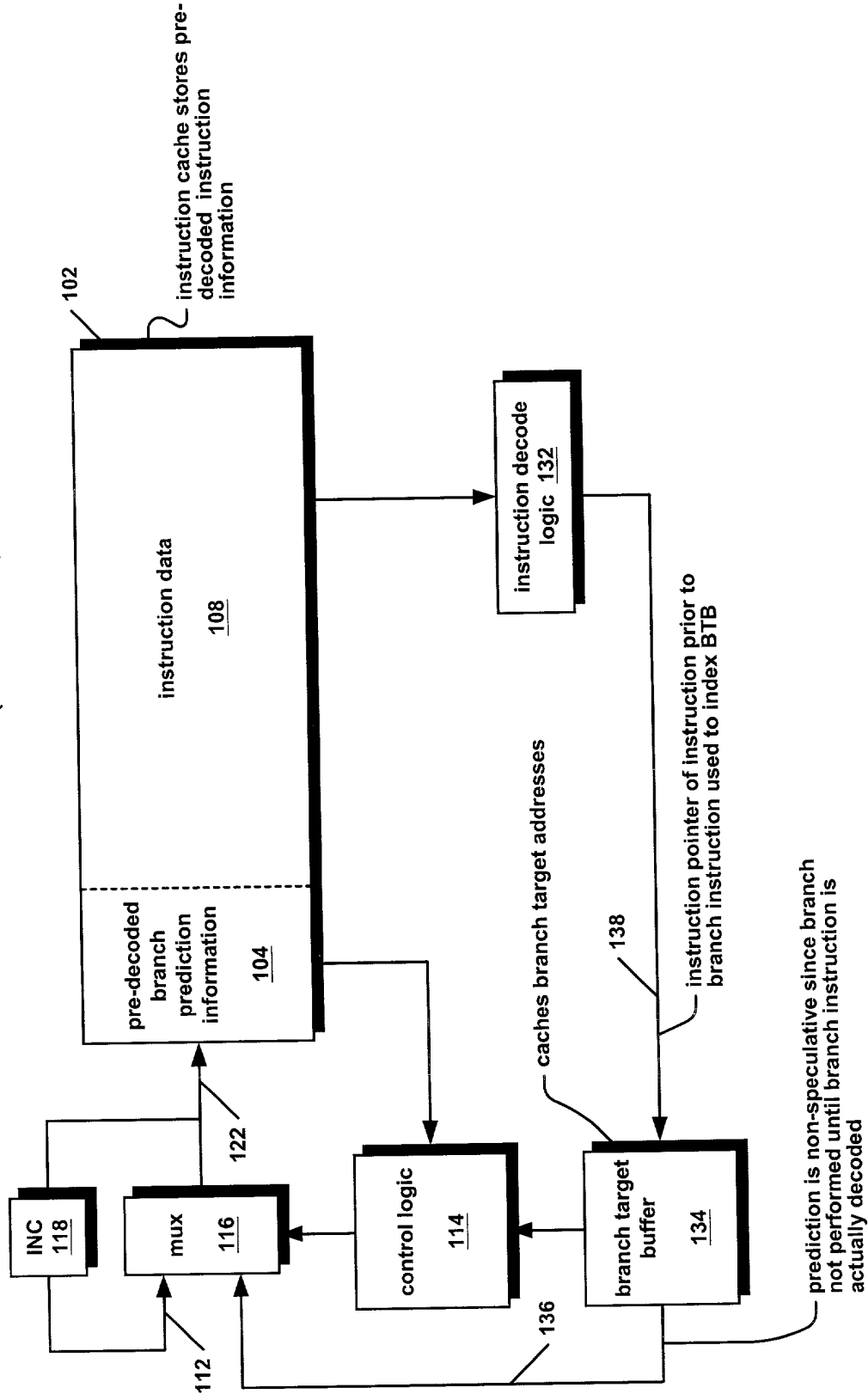


FIG. 1 (Prior Art)

FIG. 1 (Prior Art)



100

Pentium II, III Branch Target Buffer

FIG. 2 (Prior Art)

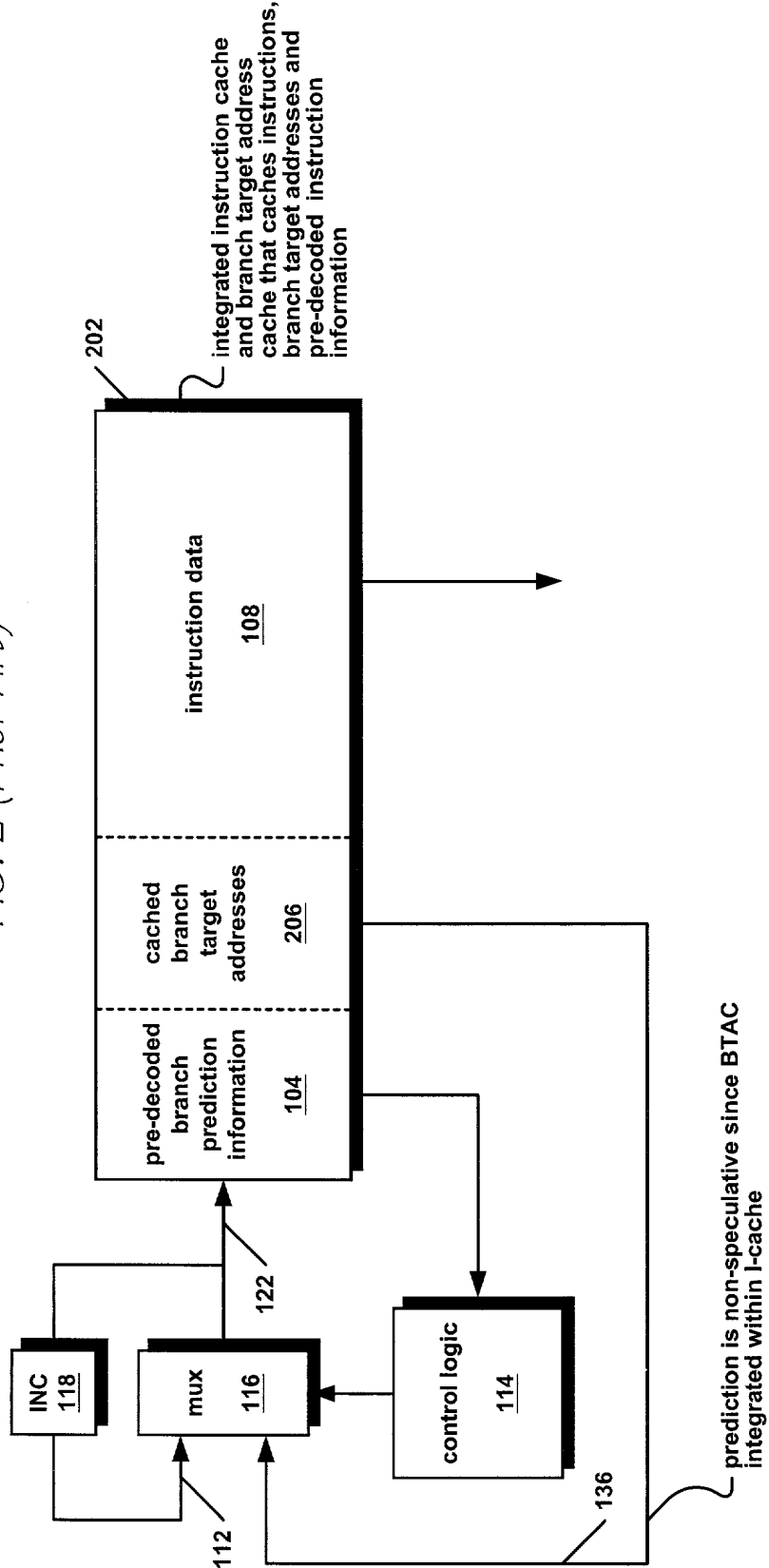
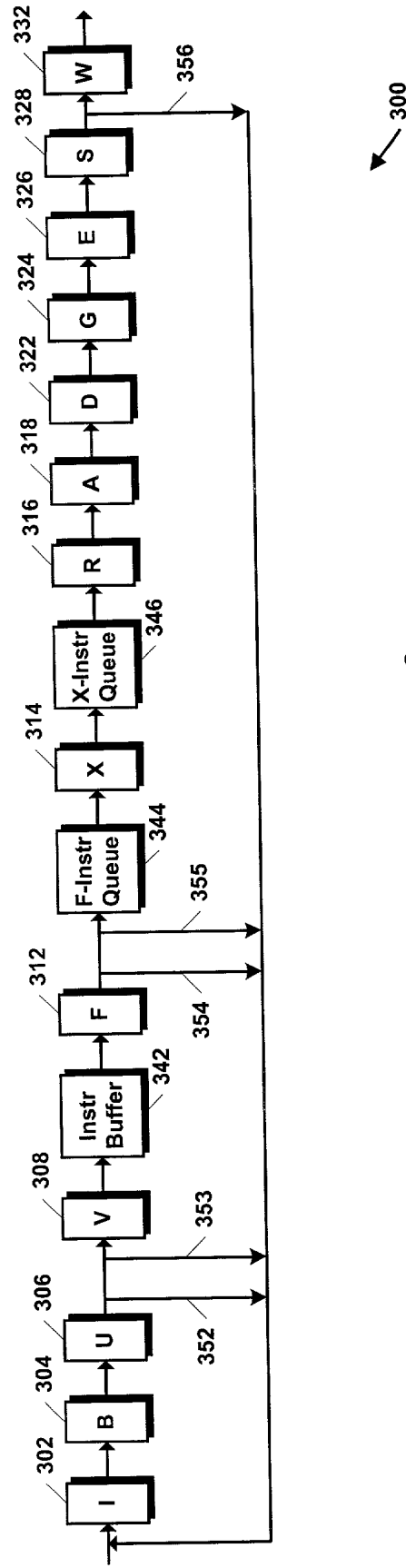
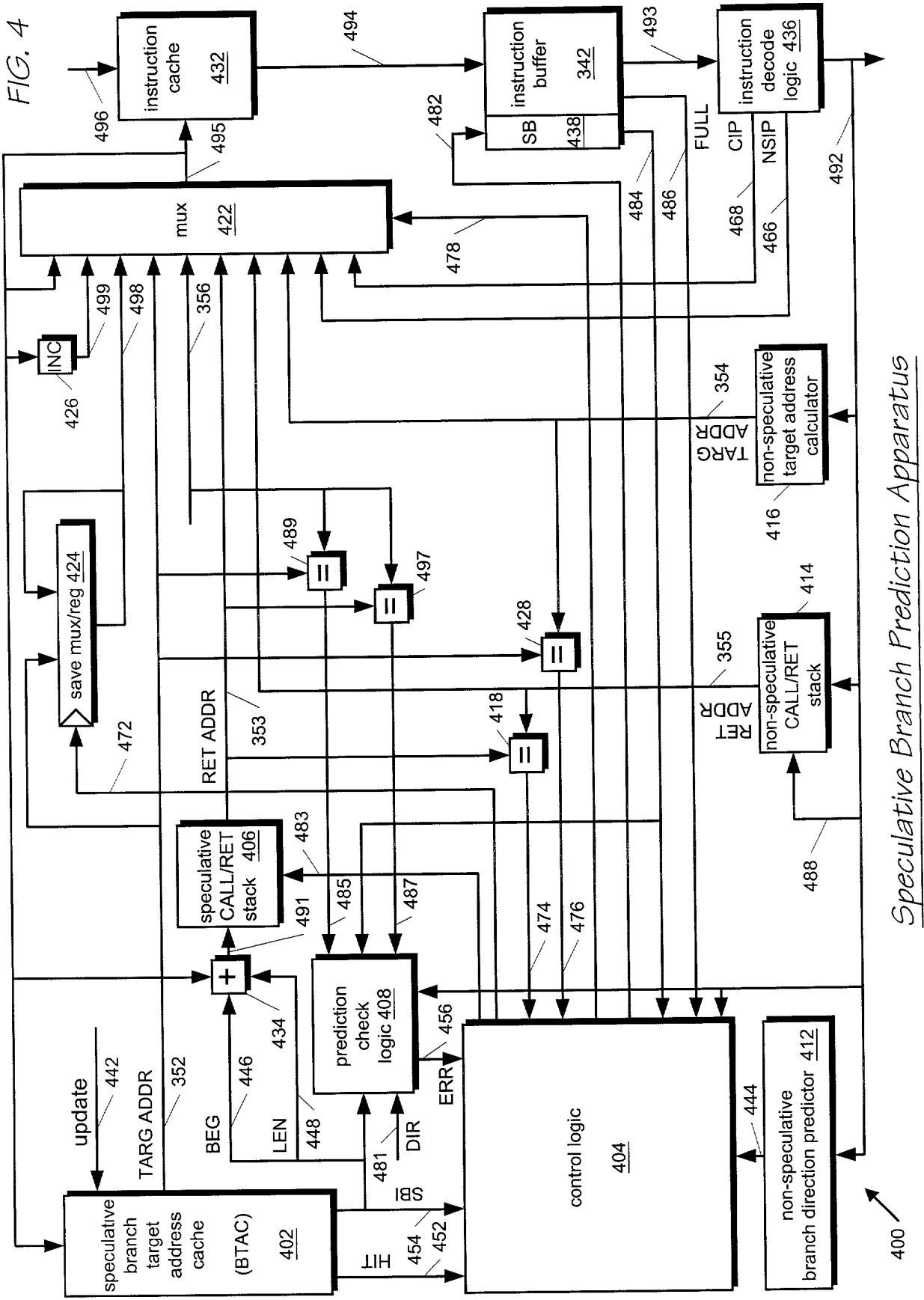


FIG. 3

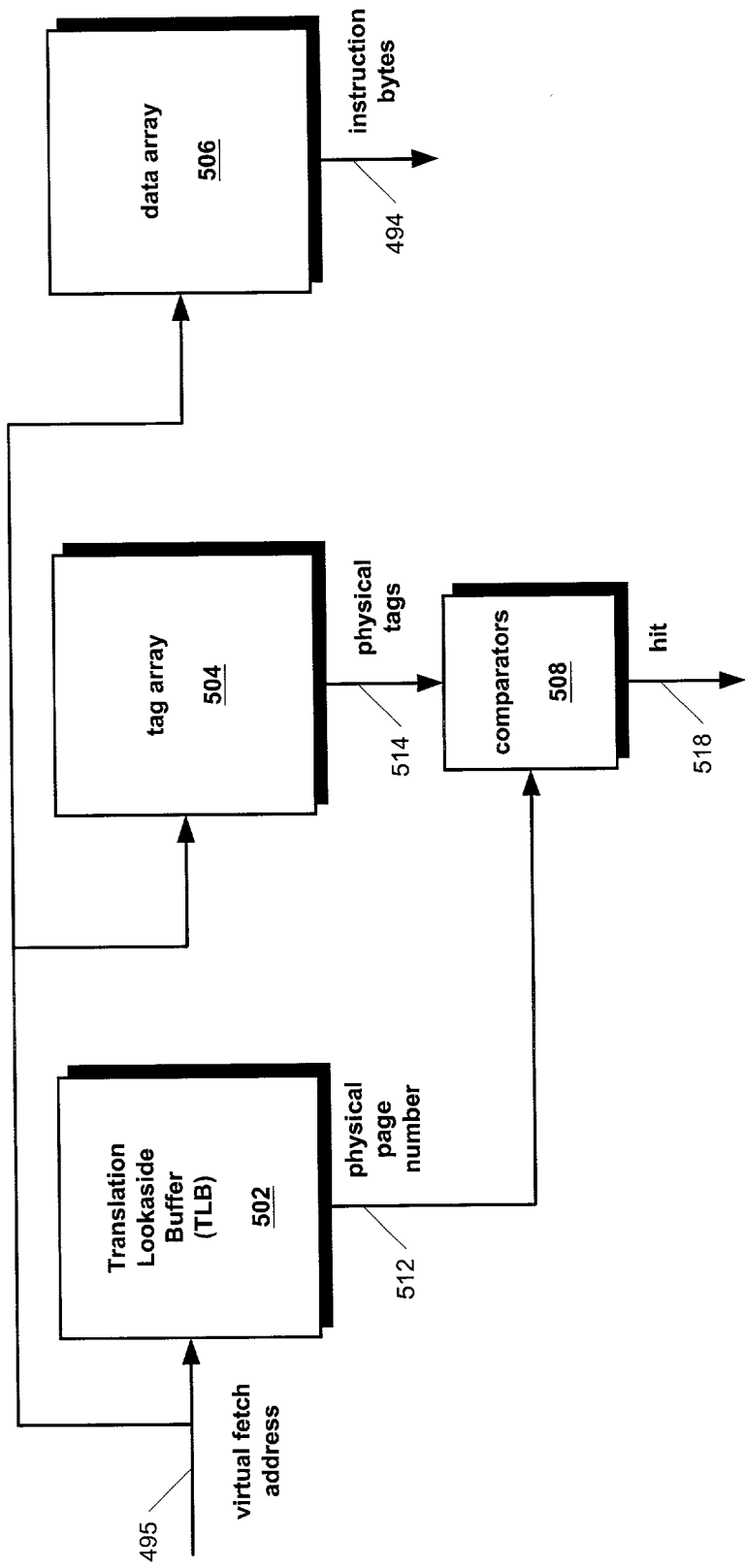


Processor Pipeline Stages



Speculative Branch Prediction Apparatus

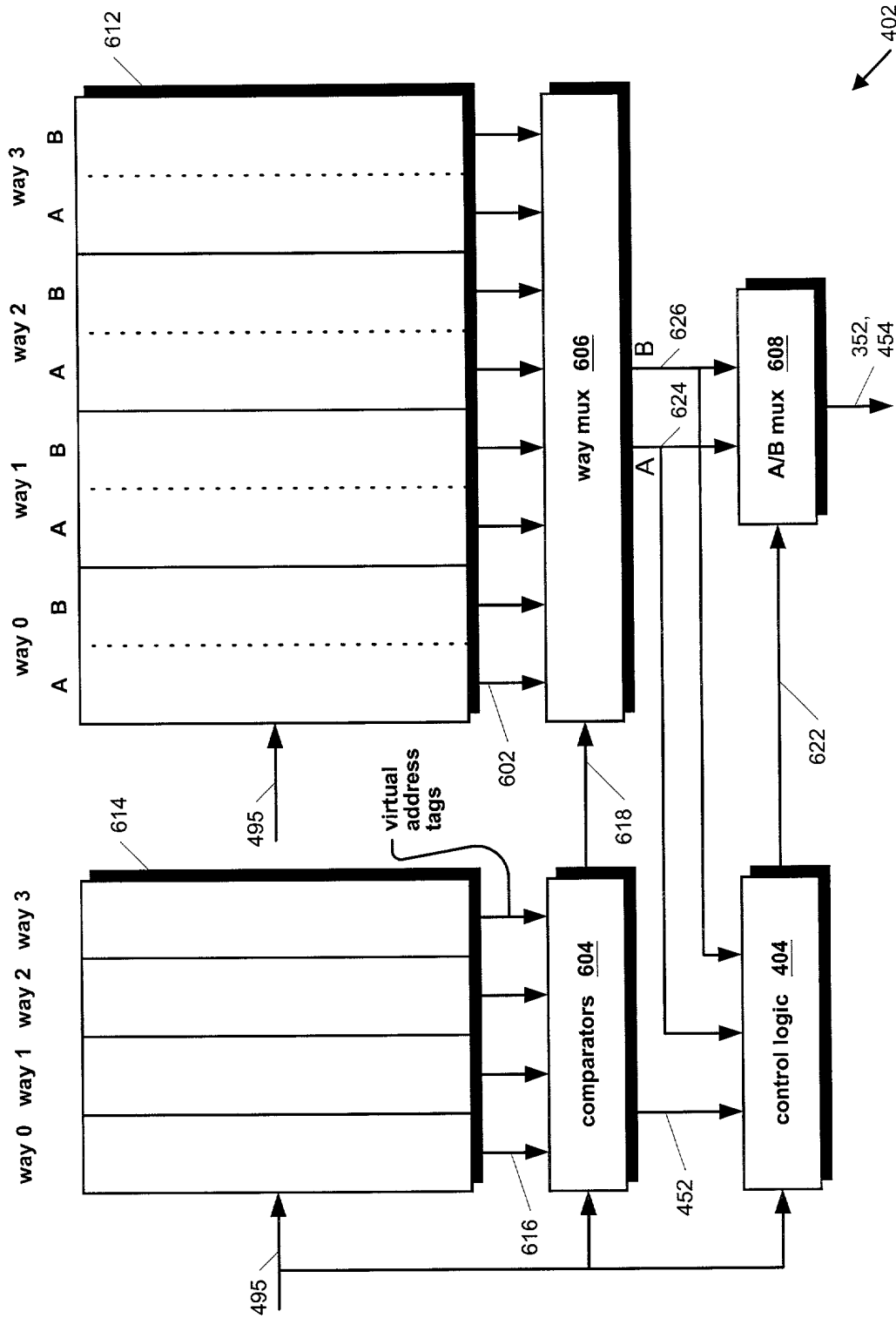
FIG. 5



Instruction Cache

FIG. 6 is a block diagram of a BTAC (Branch Target Address Cache) structure. The diagram shows a multi-ported cache structure with four ways (way 0, way 1, way 2, way 3) for both virtual address tags (612) and comparators (604). The comparators are connected to control logic (404) via a control signal (452). The comparators also output virtual address tags (618) to a way multiplexer (606). The way multiplexer outputs virtual address tags (624) to an A/B multiplexer (608). The A/B multiplexer outputs the final virtual address tags (352, 454) to the BTAC (402). The comparators are also connected to control logic (404) via a control signal (452). The comparators also output virtual address tags (618) to a way multiplexer (606). The way multiplexer outputs virtual address tags (624) to an A/B multiplexer (608). The A/B multiplexer outputs the final virtual address tags (352, 454) to the BTAC (402).

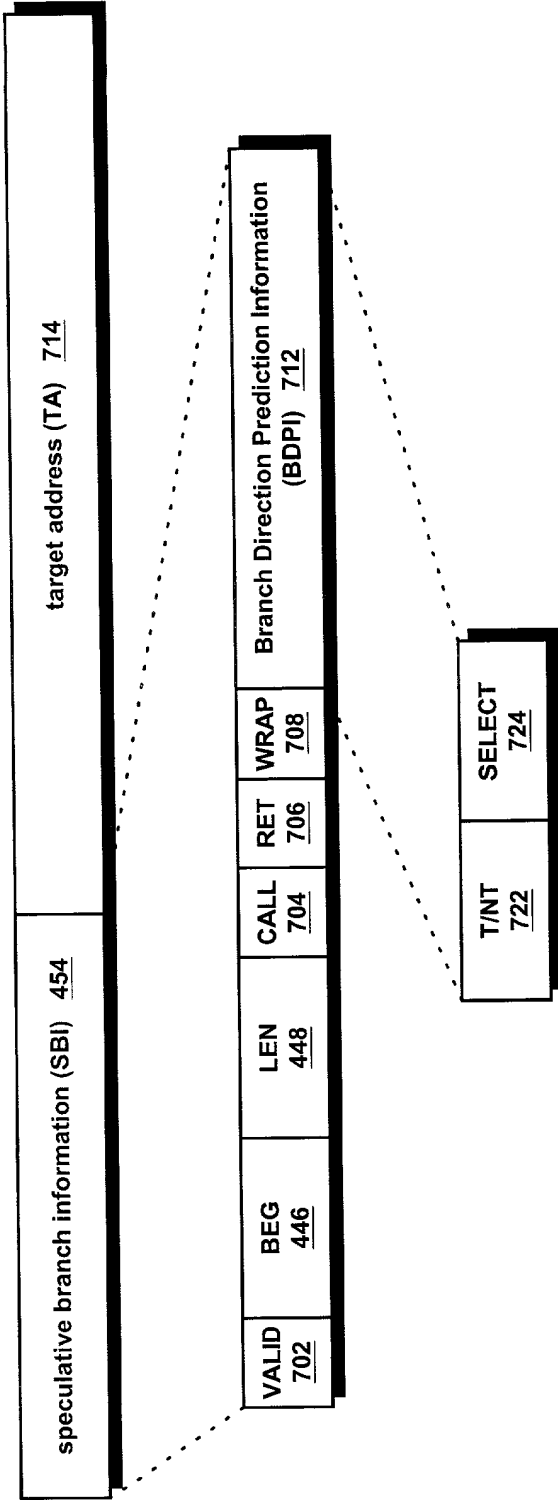
FIG. 6



BTAC

speculative branch information (SBI) 454

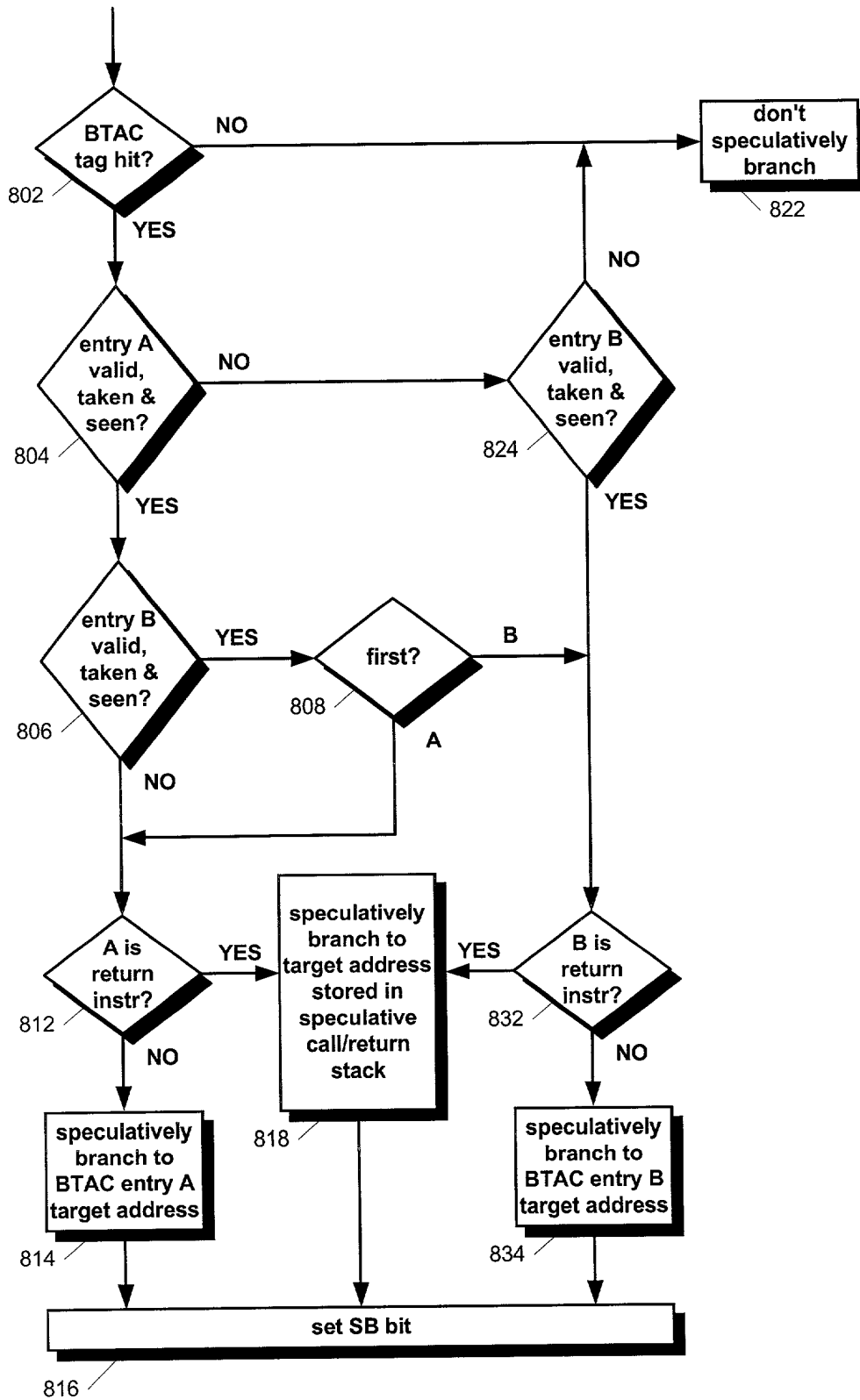
FIG. 7



602

BTAC Entry

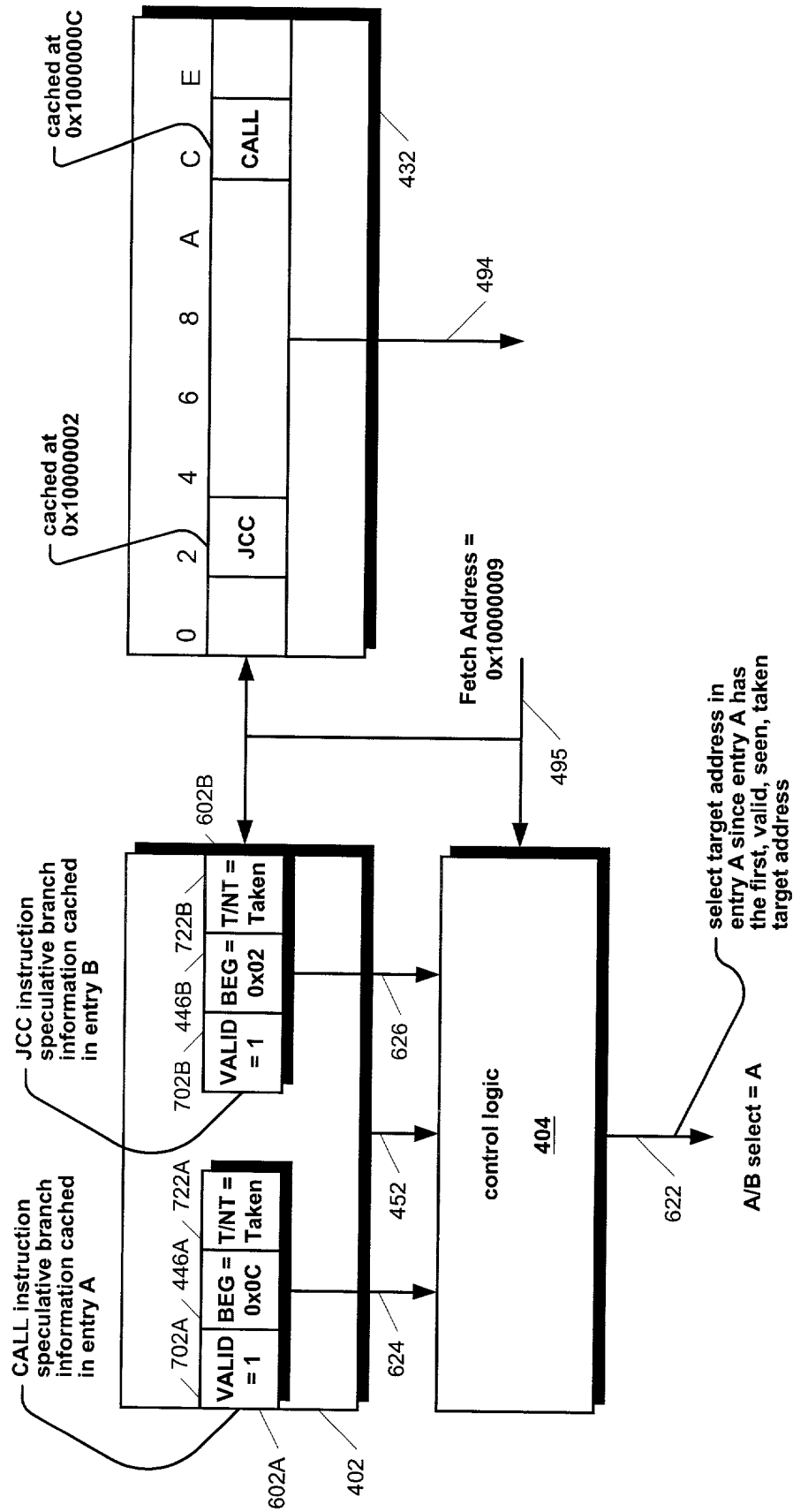
FIG. 8



Speculative Branching Operation

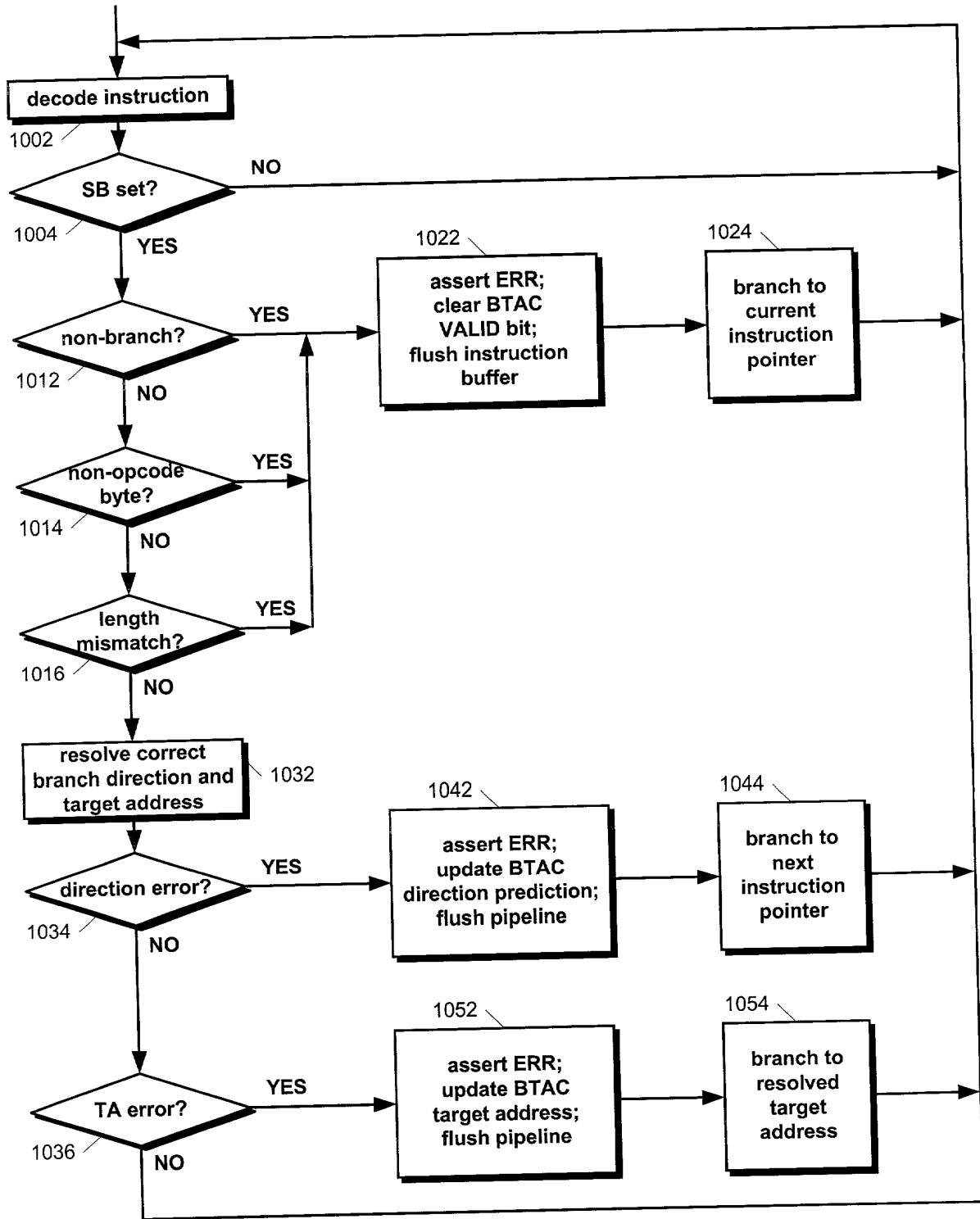


FIG. 9



Target Address Selection Example

FIG. 10



Detection and Correction of Speculative Branch Misprediction

FIG. 11

Previous Code Sequence:

0x00000010 JMP 0x00001234

...

Current Code Sequence:

0x00000010 ADD ;address 0x00000010 hits in BTAC generating a TA value of 0x00001234

...

0x00001234 SUB

0x00001236 INC

clock →	1	2	3	4	5	6	7
I-stage	ADD	X	X	SUB	INC	X	ADD
B-stage		ADD	X	X	SUB	X	X
U-stage			ADD	X	X	X	X
V-stage				ADD	X	X	X
F-stage					ADD	X	X

Cycle 1 = BTAC and I-cache access cycle

Cycle 4 = speculative branch cycle

Cycle 5 = speculative branch error detection cycle

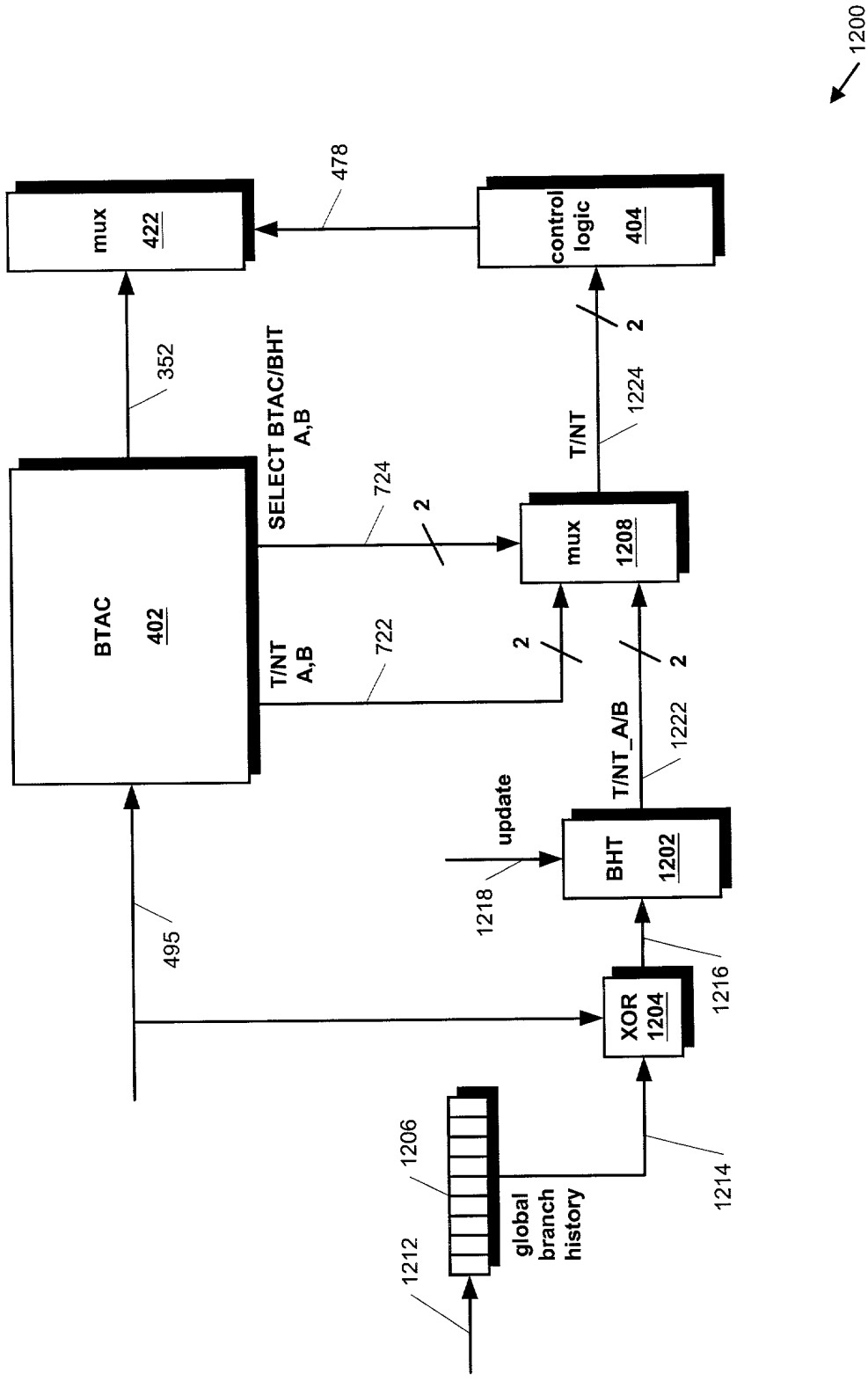
Cycle 6 = BTAC invalidate cycle

Cycle 7 = speculative branch error correction cycle

1100

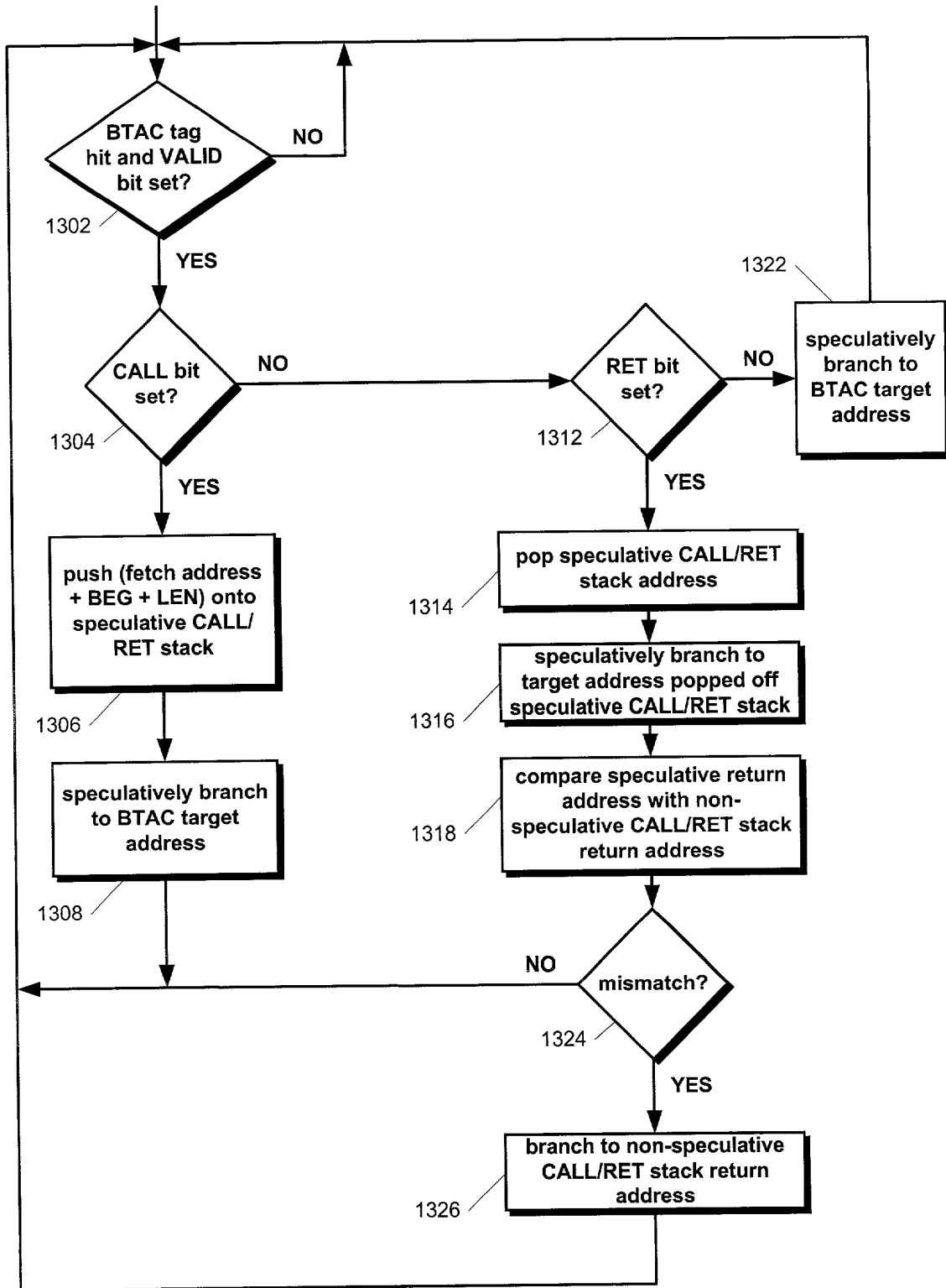
Misprediction Detection and Correction Example

FIG. 12



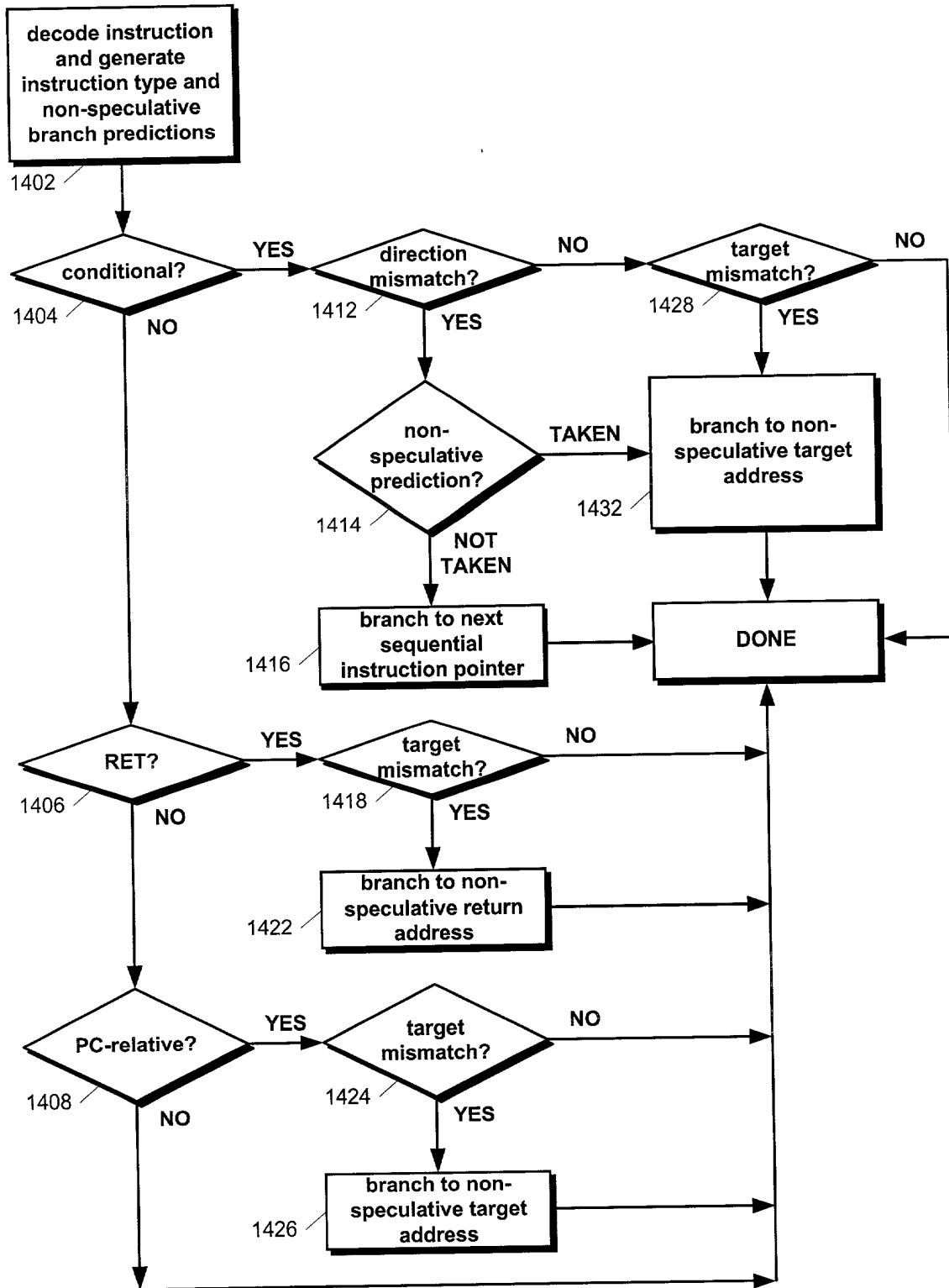
Hybrid Speculative Branch Direction Predictor

FIG. 13



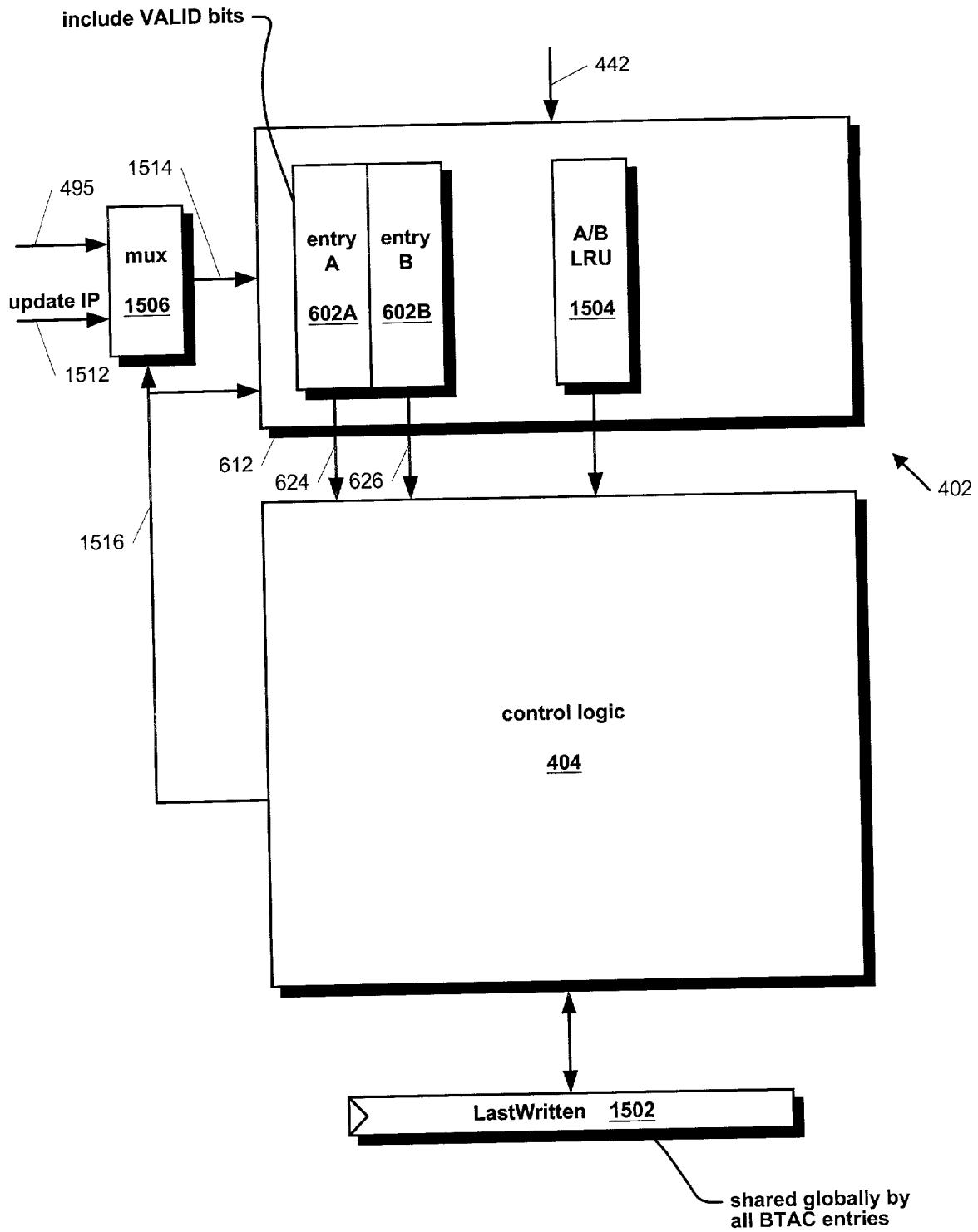
Dual CALL/RET Stack Operation

FIG. 14



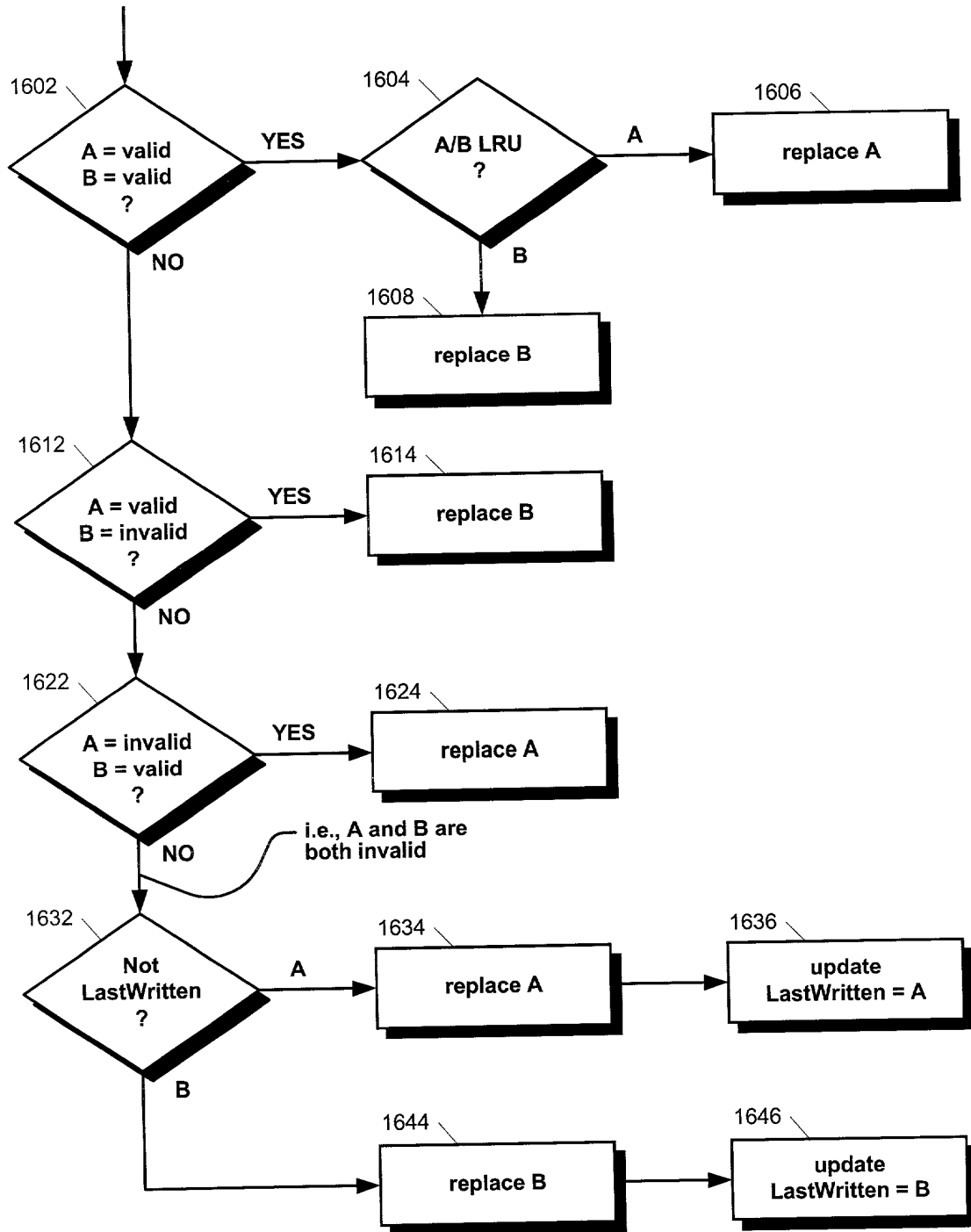
Selective Override of BTAC Prediction Operation

FIG. 15



BTAC A/B Replacement Apparatus

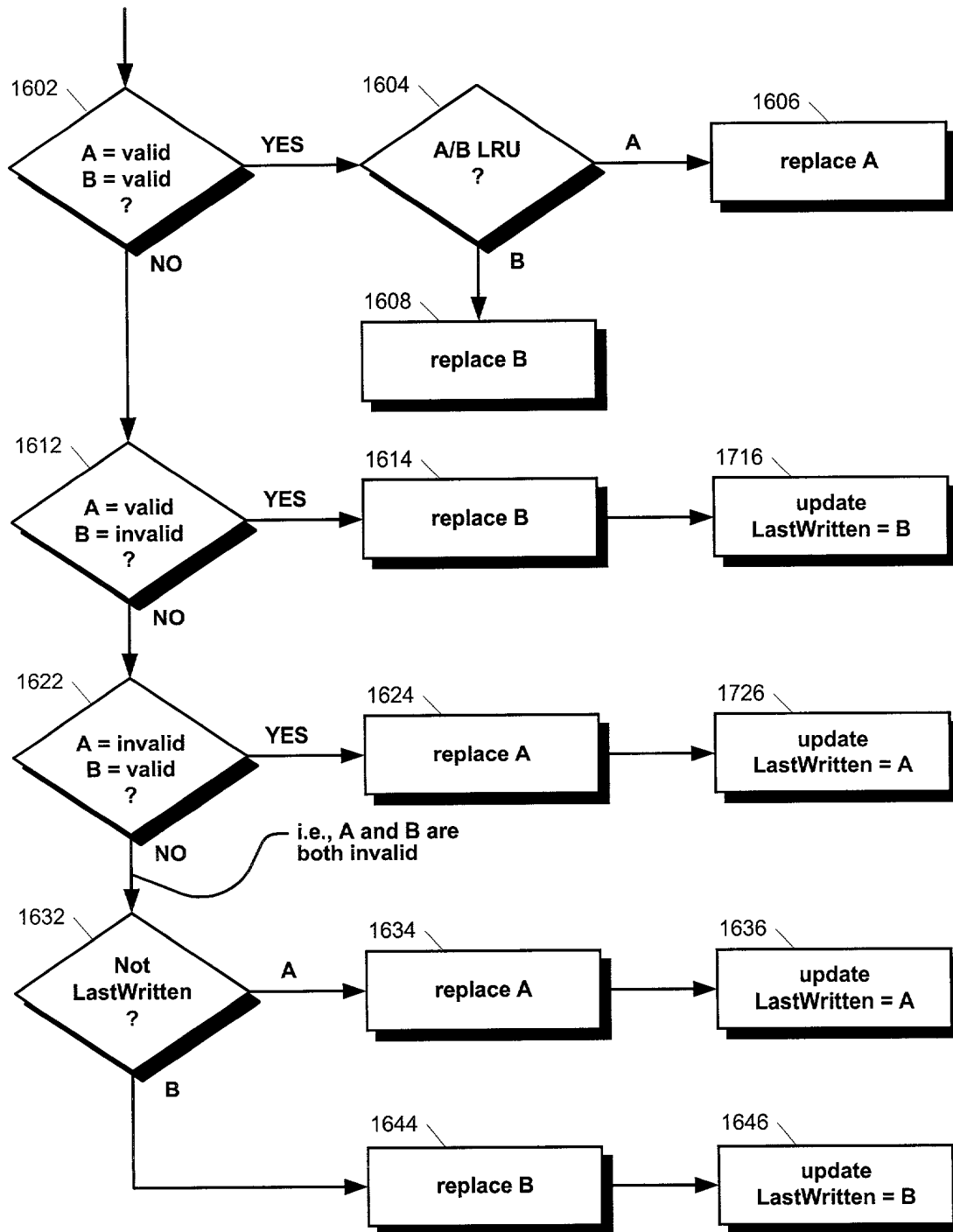
FIG. 16



A/B Entry Replacement Method

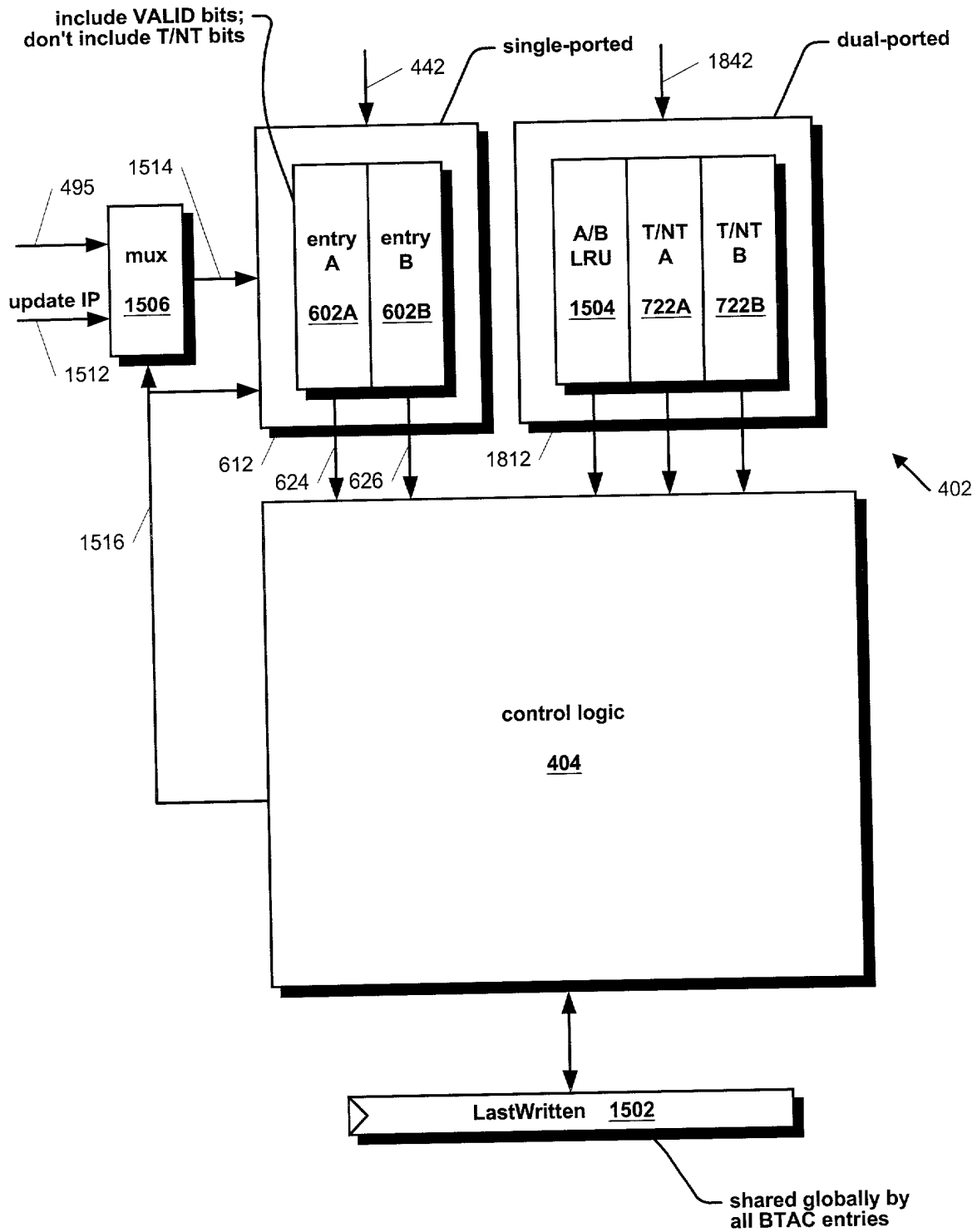


FIG. 17



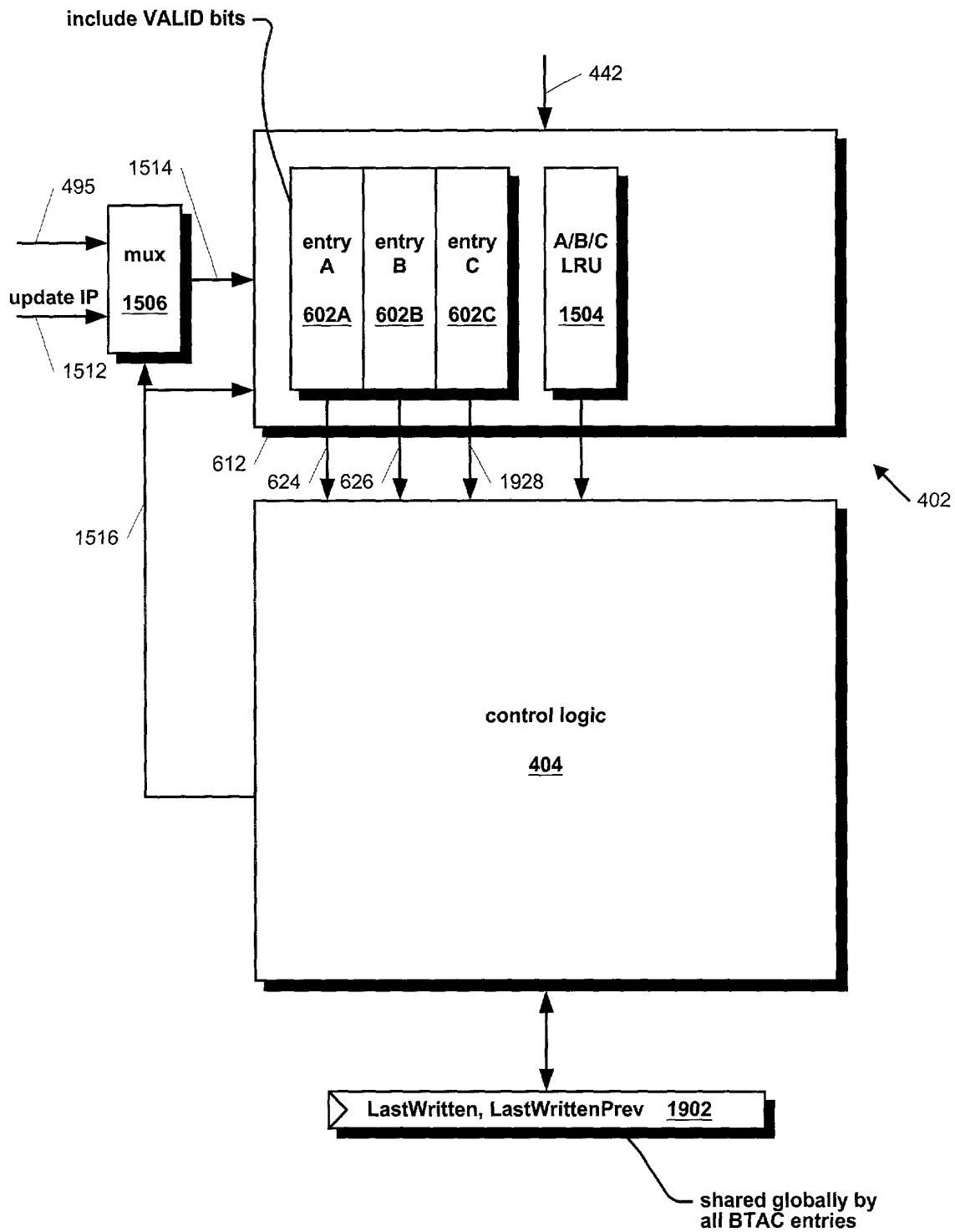
A/B Entry Replacement Method (Alt. Embodiment)

FIG. 18



BTAC A/B Replacement Apparatus (Alt. Embodiment)

FIG. 19



BTAC A/B/C Replacement Apparatus